

N THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Takashi Hoshino, et al. Art Unit : 2814
Serial No. : 10/522,278 Examiner : Mursalin B.
Filed : January 24, 2005 Hafiz
Title : VERTICAL JUNCTION FIELD EFFECT TRANSISTORS, AND
METHODS OF PRODUCING THE VERTICAL JUNCTION FIELD
EFFECT TRANSISTORS (AS AMENDED)

MAIL STOP ISSUE FEE

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Notice of Allowance Date: March 15, 2007

RESPONSE TO NOTICE OF ALLOWANCE

In response to the Notice of Allowance mailed March 15, 2007, enclosed are a completed issue fee transmittal form PTOL-85b.

The Issue and Publication fees in the amount of \$1700 are being paid concurrently herewith on the Electronic Filing System (EFS) by way of Deposit Account Authorization. Please apply any other charges or credits to Deposit Account No. 06 1050.

COMMENTS ON EXAMINER'S REASONS FOR ALLOWANCE

It is agreed that the limitations recited in the examiner's Reasons for Allowance are not taught or suggested by the art of record, and that allowed independent claim 6 is distinguished from the cited prior art for at least the reasons stated in the Reasons for Allowance. Applicants do not concede that the stated reasons are the only grounds for patentability of the allowed claims, that the limitations excluded from the Reasons for Allowance are taught or suggested by the art of record, or that all of the limitations are necessary for patentability of the allowed claims or other claims directed to the disclosed

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011US1 / FP03-0200-00US-SE(PCT)

subject matter. For example, other claims including different limitations are patentable over the cited prior art.

Respectfully submitted,

Date: May 15, 2007



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